ProJecT cLOck

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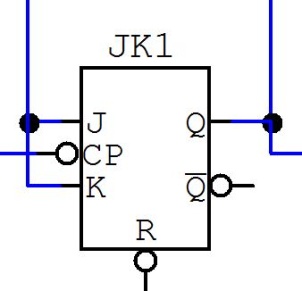
**Introduction**

Project clock is a challenge to make a digital clock circuit. Digital clock have four hex displays. The first two displays show the hour counter and the second two displays minute. The digital clock is consisted of combination of NAND gate, AND gate and J-K flip-flops. Digital clock is just a sequence of four counters mode to the flip-flops reset.

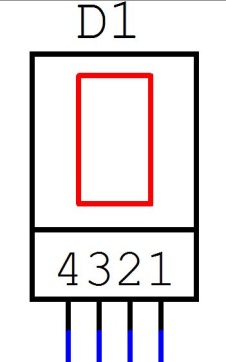
**Material**

Material needed are

* J-K flip-flop x13



* NAND x4
* AND gate x1
* Clock x1
* Switch x1
* Hex Display x13



**Procedure**

**The First Display (D1)**

The first display (**D1**) is a hex display with 4 inputs labeled by **1**, **2**, **3** and **4**. The function of **D1** is to display the second digit of minute counter 0 up to 9, therefore to make that works we need 4 flip-flops because we need to show 4 bit number. The 4 flip-flops will be “:

→ The first J-K flip-flop **JK1**‘s **J** and **K** will input switch **A** and **CP** will take the output of the **CLK**. The output of the **JK1**’s **Q** will be connected to both the **JK2**’s **CP** and the **D1** no ‘**1**’ labeled input.

→ The second J-K flip-flop **JK2**‘s **J** and **K** will input switch **A** and **CP** will take the **JK1** ‘s **Q**. The output of the **JK2**’s **Q** will be connected to both the **JK3**’s **CP** and **D1** no ‘**2**’ labeled input.

→ The third J-K flip-flop (**JK3**)‘s **J** and **K** will input switch **A** and **CP** will take **JK2** ‘s **Q**. The **JK3**’s **Q** will be connected to both the **JK4**’s **CP** and **D1** no ‘**3**’ labeled input.

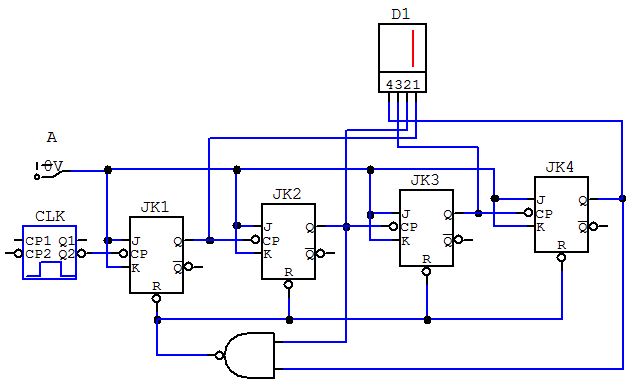
→ The fourth J-K flip-flop (**JK4**)‘s **J** and **K** will input switch **A** and **CP** will take **JK3** ‘s **Q**. The output of the **JK4**’s **Q** will be connected to both the **JK5**’s **CP** and **D1** no ‘**4**’ labeled input.

This serious connection of J-K flip-flop will only count (**0** - **F**) but it should count up to 9, we have to make it reset at 10.

The **D1** displays 10(**A**). Since **D1** is inputs are binary 10(A) is 1010 which means when **JK4** and **JK2** are **1**. So we connect the output of the **JK4**’s **Q** and **JK2**’s **Q** with **NAND** gate (**ND1**) to the connection of **R**’s of **JK1**, **JK2**, **JK3** and **JK4**.

So **D1** after 9 clock’s display 9 and when the tenth clock comes **JK2** and **JK4** will be 1 and the reset will be 0, therefore it will reset and will count start from 0.

* All flip-flop J and K will input switch A
* All flip-flop R will be connected to JK2 and JK4 Q output



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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Truth table for the Hex display D1** | | | | | | | | | | | | | | |
| CLK | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| Hex Display  **D1** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **0** | **1** | **2** | **3** |

**The Second Display (D2)**

The Second display (**D2**) is a hex display with 3 inputs labeled by **1**, **2** and **3**. The function of **D2** is to display the first digit of minute counter 0 up to 5, therefore to make that works we need 3 flip-flops because we need to show 3 bit number. The 3 flip-flops will be assembled like written below.

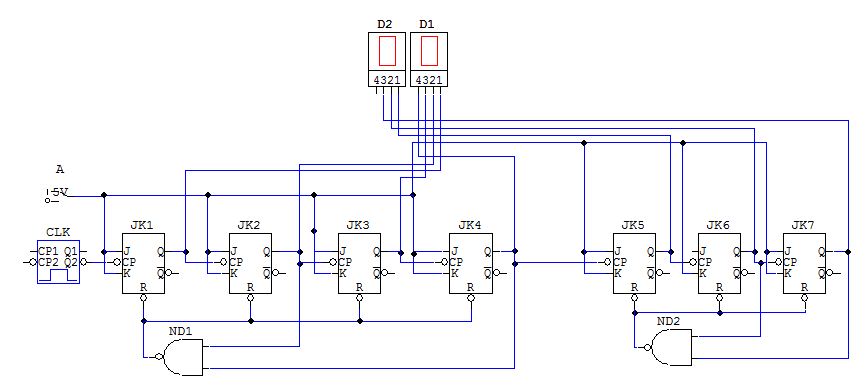
→ The fifth J-K flip-flop **JK5**‘s **J** and **K** will input switch **A** and **CP** will take the **JK4** ‘s **Q**. The output of the **JK5**’s **Q** will be connected to both the **JK6**’s **CP** and **D2** no ‘**1**’ labeled input.

→ The sixth J-K flip-flop (**JK6**)‘s **J** and **K** will input switch **A** and **CP** will take **JK5** ‘s **Q**. The **JK6**’s **Q** will be connected to both the **JK7**’s **CP** and **D2** no ‘**2**’ labeled input.

→ The seventh J-K flip-flop (**JK7**)‘s **J** and **K** will input switch **A** and **CP** will take **JK6** ‘s **Q**. The output of the **JK7**’s **Q** will be connected to both the **JK8**’s **CP** and **D2** no ‘**3**’ labeled input.

This serious connection of J-K flip-flop will only count (**0** - **F**) but it should count up to 5, we have to make it reset at 6.

The **D2** displays ‘**6**’. Since **D2** is inputs are binary 6 is 110 which means when **JK6** and **JK7** are **1**. So we connect the output of the **JK6**’s **Q** and **JK7**’s **Q** with **NAND** gate (**ND2**) to the connection of **R**’s of **JK5**, **JK6** and **JK7**.



|  |  |
| --- | --- |
| **Truth table of Hex display D2** | |
| JK4’s Q Output (NGT) | Hex display |
| 0 | **0** |
| 1 | **1** |
| 2 | **2** |
| 3 | **3** |
| 4 | **4** |
| 5 | **5** |
| 6 | **0** |
| 7 | **1** |
| 8 | **2** |
| 9 | **3** |

**The Third Display (D3)**

The third display (**D3**) is a hex display with 4 inputs labeled by **1**, **2**, **3** and **4**. The function of **D3** is to display the second digit of hour counter 0 up to 9, therefore to make that works we need 4 flip-flops because we need to show 4 bit number. The 4 flip-flops will be assembled like written below.

→ The eighth J-K flip-flop **JK8**‘s **J** and **K** will input switch **A** and **CP** will take the **JK7** ‘s **Q**. The output of the **JK8**’s **Q** will be connected to both the **JK9**’s **CP** and **D3** no ‘**1**’ labeled input.

→ The ninth J-K flip-flop (**JK9**)‘s **J** and **K** will input switch **A** and **CP** will take **JK8** ‘s **Q**. The **JK9**’s **Q** will be connected to both the **JK10**’s **CP** and **D1** no ‘**2**’ labeled input.

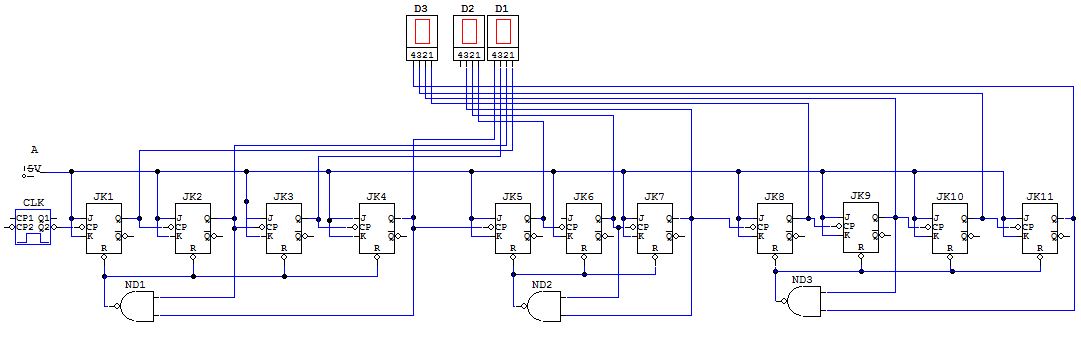
→ The tenth J-K flip-flop (**JK10**)‘s **J** and **K** will input switch **A** and **CP** will take **JK9** ‘s **Q**. The output of the **JK10**’s **Q** will be connected to both the **JK11**’s **CP** and **D3** no ‘**3**’ labeled input.

→ The eleventh J-K flip-flop (**JK11**)‘s **J** and **K** will input switch **A** and **CP** will take **JK10** ‘s **Q**. The output of the **JK11**’s **Q** will be connected to both the **JK12**’s **CP** and **D3** no ‘**4**’ labeled input.

This serious connection of J-K flip-flop will only count (**0** - **F**) but it should count up to 9, we have to make it reset at 10.

The **D3** displays 10(**A**). Since **D3** is inputs are binary 10(A) is 1010 which means when **JK9** and **JK11** are **1**. So we connect the output of the **JK9**’s **Q** and **JK11**’s **Q** with **NAND** gate (**ND3**) to the connection of **R**’s of **JK8**, **JK9**, **JK10** and **JK11**.

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| **Truth table of Hex display D3** | |
| JK7’s Q Output (NGT) | Hex display |
| 0 | **0** |
| 1 | **1** |
| 2 | **2** |
| 3 | **3** |
| 4 | **4** |
| 5 | **5** |
| 6 | **6** |
| 7 | **7** |
| 8 | **8** |
| 9 | **9** |
| 10 | **0** |
| 11 | **1** |
| 12 | **2** |
| 13 | **3** |



**The Fourth Display (D4)**

The Fourth display (**D4**) is a hex display with 2 inputs labeled by **1** and **2**. The function of **D4** is to display the first digit of hour counter 0 up to 2, therefore to make that works we need 2 flip-flops because we need to show 2 bit number. The 2 flip-flops will be assembled like written below.

→ The twelve J-K flip-flop (**JK12**)‘s **J** and **K** will input switch **A** and **CP** will take **JK11** ‘s **Q**. The **JK12**’s **Q** will be connected to both the **JK13**’s **CP** and **D4** no ‘**1**’ labeled input.

→ The tenth-third J-K flip-flop (**JK13**)‘s **J** and **K** will input switch **A** and **CP** will take **JK12** ‘s **Q**. The output of the **JK13**’s **Q** will be connected to **D4** no ‘**2**’ labeled input.

After making this, our circuit will count up to **39:59** but our hour counter should reset at 23:59 which means we have two conditions to reset the **D3** hour counters

1. When the second hour display reaches 9 ***Reset the D3***
2. When the second hour display **D3** reaches 4 and at the same time the first hour display **D4** reaches 2 ***Reset the both D3 & D4***

So we have to modify our circuit and make it applicable for our conditions!

@condition 1: Since **D3** is inputs are binary 10(A) is 1010 which means when **JK9** and **JK11** are **1**. So we connect the output of the **JK9**’s **Q** and **JK11**’s **Q** with **NAND** gate (**ND3**) to the connection of **R**’s of **JK8**, **JK9**, **JK10** and **JK11**. As written above.

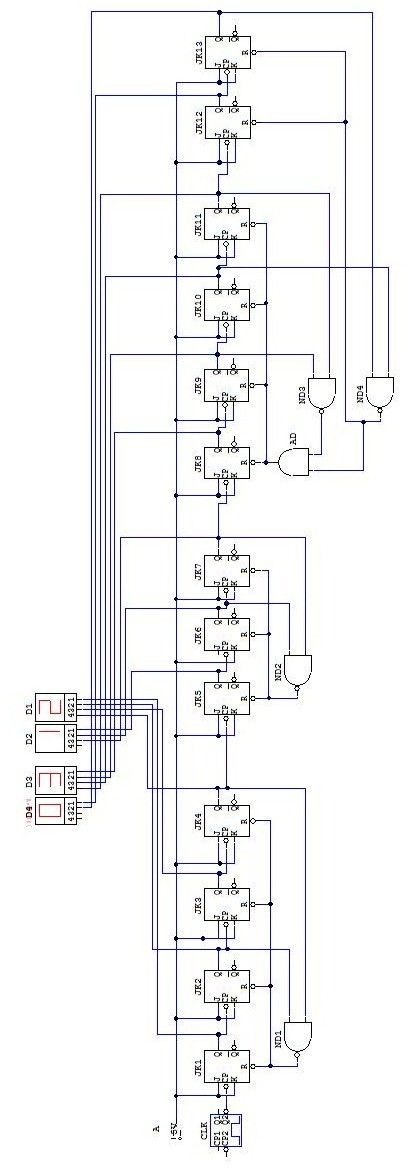
@condition 2: The output of **D3** when it become **4** is 100 and the output for **D4** when it become **2** is 10, therefore we connect **JK10**’s and **JK13**’s **Q** and connect with NAND gate (**ND4**) them with to both **AD** and **JK12** and **JK13**’s **R**.

Then we connect both conditions with an And gate **AD**!

Now our hour circuit can count up to **09** and **D3** reset but **D4** become **1**

So they will display **10**, when our circuit becomes **19** and on the next **CLK** the **D3** and **D4** becomes **2**.

Finally when the clock become **23:59** on the next **CLK** all **D1**,**D2**,**D3** and **D4** reset!



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| --- | --- | --- |
| **Truth table for the Hour Display** | | |
| Input for hour (NGO) | D4 | D3 |
| 0 | **0** | **0** |
| 1 | **0** | **1** |
| 2 | **0** | **2** |
| 3 | **0** | **3** |
| 4 | **0** | **4** |
| 5 | **0** | **5** |
| 6 | **0** | **6** |
| 7 | **0** | **7** |
| 8 | **0** | **8** |
| 9 | **0** | **9** |
| 10 | **1** | **0** |
| 11 | **1** | **1** |
| 12 | **1** | **2** |
| 13 | **1** | **3** |
| 14 | **1** | **4** |
| 15 | **1** | **5** |
| 16 | **1** | **6** |
| 17 | **1** | **7** |
| 18 | **1** | **8** |
| 19 | **1** | **9** |
| 20 | **2** | **0** |
| 21 | **2** | **1** |
| 22 | **2** | **2** |
| 23 | **2** | **3** |
| 24 | **0** | **0** |
| 25 | **0** | **1** |
| 26 | **0** | **2** |
| 27 | **0** | **3** |
| 28 | **0** | **4** |